A Time-to-Digital Converter Based on Time-Space Relationship

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Abstract—**This paper describes a time-to-digital converter based on time-space relationship to improve the measuring precision of time interval. A tapped transmission line of certain length is used as the delay line, which converts the measured time to length. The delay characteristics and electrical performance of two types of transmission lines, coaxial cable and microstrip, are analyzed, as well as the factors affecting the delay characteristics, such as loss and temperature. The coincidence detection of the delayed start signal and stop signal is so critical that a type of coincidence detection circuit is developed, of which the uncertainty is 14ps. Buffer is used to enlarge the measurement range. The structure of the time-to-digital converter is also presented, of which the quantization error, integral nonlinearity error and random error is analyzed. An advantage of this kind of time-to-digital converter is easy to be integrated. Based on the CMOS technology, a chip is designed, and a simulation of the chip is performed, which presents 23ps single-shot precision. As a demonstration of this principle, a prototype using the microstrip on a printed-circuit-board as delay line is realized with 108ps single-shot precision.**

I. INTRODUCTION

High-precision time interval measurement systems are commonly used in various applications, such as navigation, positioning, laser ranging and so on. Time interval digitization with picosecond resolution using only a simple counter requires impractically high clock frequencies or long averaging times. To overcome this, various interpolation methods are used to improve the resolution, including analog and digital techniques [1]. As the development of IC, an interpolation method easy to be integrated is to use logic-element delays or the delay difference between logic elements to create a tapped delay line, which is then used to interpolate the time fractions inside the clock cycle.

In order to further improve the resolution, a finer delay unit should be developed for quantization. Since the signal traveling in the transmission line is of high speed and stability, the time-space relationship has been used for measurement of time interval [2] [3]. A tapped transmission line of certain length is used as the delay line, which converts the measured time to length. Input to the starting point of the delay line the start signal is delayed by the tapped transmission lines and gets coincident with the stop signal. By this means, the time is converted to length, that is, the time interval is equal to the total delay of the tapped transmission lines between the coincidence point and the starting point, and the resolution is equal to the delay of unit tapped transmission line, which is easy to be of the order of picosecond.

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II. DELAY CHARACTERISTICS OF TRANSMISSION LINE

A. Delay Characteristics of Ideal Transmission Line

Ideal transmission line is lossless, i.e., the traveling voltage wave at all points along the line has the same amplitude. Based on the transmission line equation, the propagation delay per unit length t_d is described as,

$$t_d = \sqrt{LC} \tag{1}$$

Where L is the inductance per unit length, and C is the capacitance per unit length.

B. Factors Affecting Performance of Propagation Delay

The ideal transmission line is not practical. Realistically, various factors affect the delay characteristics, such as loss, temperature, etc.. A detailed analysis is followed.

1) Loss: A important factor affecting the delay is loss, including resistive and dielectric loss. The lossy line behaves like a combination of inductance-capacitance and resistance-capacitance line [4]. In the case when $Rl \le 0.1Z_0$, the interconnect transmission lines are considered lossless and distortionless. The LC model can be used to predict the delay. This is the case for the microchip on printed circuit board. In the case when $Rl > 2Z_0$, the lines are much more resistive, whose delays should be estimated using RC or RLC models. This is the case for on-chip wiring. The Elmore model [5] is widely used to predict the delay in chip design. As the frequency increases or the transition time becomes faster, the coupling capacitance and the inductance should also be considered.

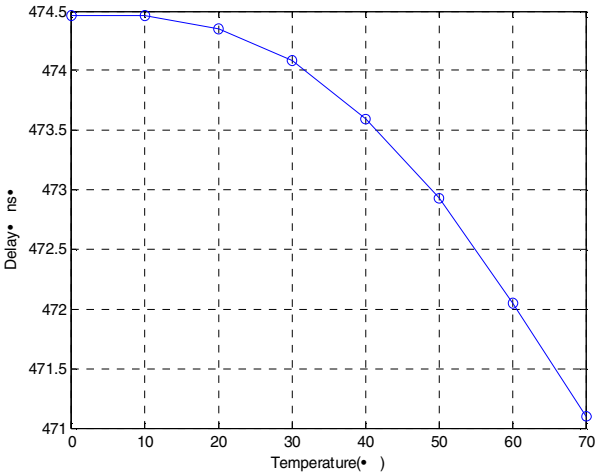


Figure 1. Delay characteristic of a 93-m coaxial cable

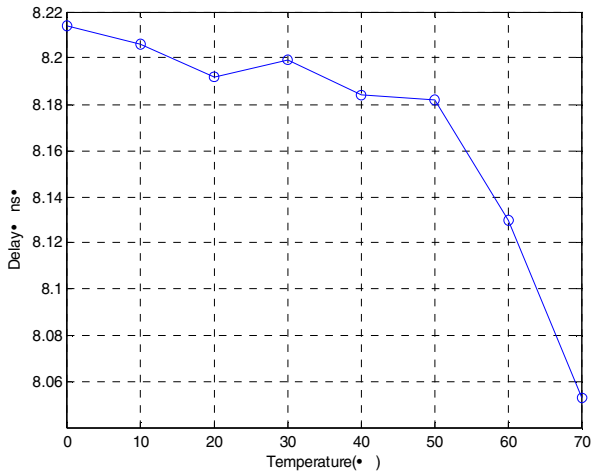


Figure 2. Delay characteristic of a 1-m microstrip on PCB

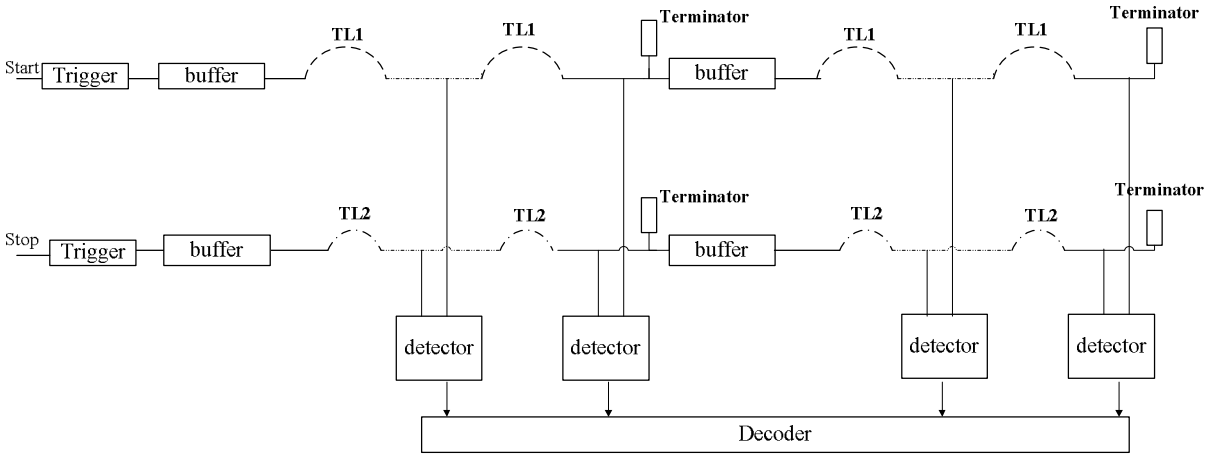


Figure 3. Block diagram of TDC

2) Temperature: Since the dielectric constant changes with temperature, the delay of a transmission line is dependent on the temperature. To find out the relationship of the delay and the temperature, an experiment is done, in which the delay characteristics of a coaxial cable and a microstrip are measured. Fig.1 shows the delay of 93.2-mm coaxial cable versus temperature from 0℃ to 70℃, while Fig.2. shows that of microstrip. From the plots, the variation of delay with temperature is less than 0.005ps/℃ and 0.037ps/℃ for a 1-cm coaxial cable and a 1-cm microstrip, respectively.

III. Design of TDC in CMOS Technology

A. Structure of TDC

The block diagram of the TDC is presented in Fig.3. The start and stop signals of the measured time interval are input to the start trigger and stop trigger, respectively, by which both are converted to pulse signals with sharp rising edge of about 1ns. Then the pulse signals are buffered, since the following delay line and coincidence detections circuit are such a heavy load. The start signal and stop signal are delayed by TL1 and TL2, respectively, while both are attenuated due to the loss. In order to enlarge the measurement range, both are regenerated by buffers of identical configuration. The delayed start signal and stop will get coincident as TL1>TL2, then the measured time interval is converted to length. The statuses of coincidence detection circuits are latched. The measured time interval is decoded from the statuses.

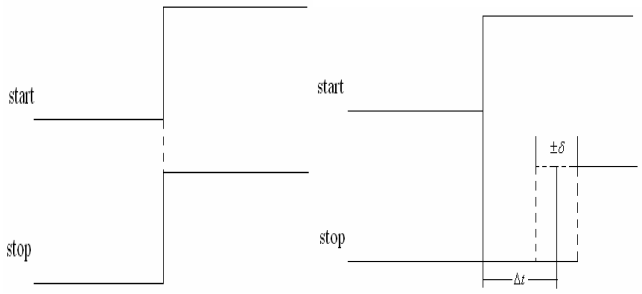
B. Coincidence Detection Circuit

The position of coincidence reflects the value of the time interval. The ideal coincidence position, as shown in Fig. 4(a), is defined as where the rising edges of delayed start signal and stop signal get coincident. The function of the ideal coincidence detection circuit is to detect the ideal coincidence, and to present a coincidence signal. In reality, the coincidence signal is presented when a time difference Δt, as shown in Fig. 4(b), exists between the delayed start signal and the stop signal when the coincidence signal is presented. Since the coincidence detection circuits are affected by many factors, such as noise, mismatches and so on, differences also exist in the circuits, which are of the same structure. So the time

difference must be $\Delta t \pm \delta$. Hereby δ is defined as the uncertainty of the coincidence detection circuit, while Δt can be corrected as a system error. A coincidence detection circuit similar to the edge-triggered flip-flop is designed for the TDC. The block diagram [5] is shown in Fig. 5. The aspect ratio of the CMOS transistors is elaborately designed. For testing the performance of the coincidence detection circuit, the SPICE model and the corner model is used to predict Δt and δ defined above in the simulation of the circuit. In the typical corner model, Δt is measured to be 400ps, while in the case of fast model and slow model (3σ model), Δt is measured to be 440ps and 480ps, respectively. Therefore, it can be calculated that $\Delta t = 400\,ps$ and $\delta = 14\,ps$.

C. Buffer

The start signal and stop signal are delayed by TL1 and TL2, the vernier, respectively, while both are attenuated due to the loss. In order to enlarge the measurement range, both are regenerated by buffers of identical configuration. The block diagram [5] is shown in Fig. 6. Ideally, the delays of both are identical. However, difference exists between both buffers due to various factors, such as mismatch and tolerance. The difference is a component of system error, which should be corrected.



(a) (b)

Figure 4. (a) Ideal coincidence (b) The definition of Δt and δ

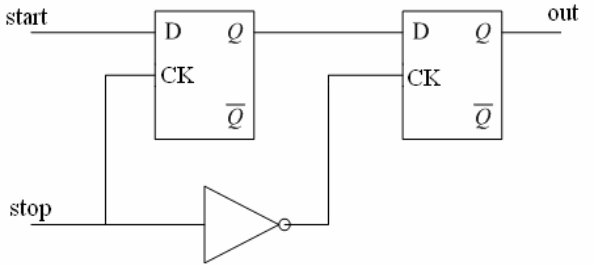


Figure 5. Coincidence detection circuit

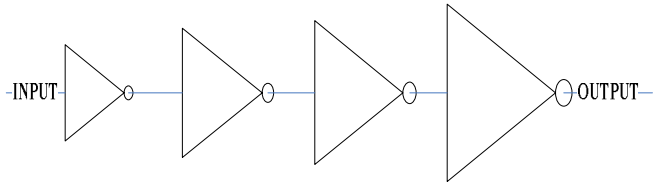


Figure 6. Block diagram of buffer

IV. Error Analysis

The performance of a TDC is generally evaluated by the single-shot precision, which is the capability of resolving the time interval of a time digitizer. It is defined as the standard deviation of the distribution of the measurement results around the mean value when a single time interval is measured repeatedly [6]. The following errors are the main components of the single-shot precision.

A. Quantization Error

Quantization error in a time measurement system is caused by the finite interpolation resolution. The random error due to quantization can be expressed by the standard deviation of the related binomial probability distribution [1]

$$\sigma = T_0 \sqrt{F(1-F)} \tag{2}$$

The maximum value is $\sigma_{\max} = T_0/2$ obtained at $F = 0.5$. The rms value can be found by integral of the function $\sigma^2(F)$ within the bounds $0 \le F \le 1$,

$$\sigma_{rms} = T_0 / \sqrt{6} \tag{3}$$

The length of time interval can be presented in terms of the LSBs.

B. Integral Nonlinearity Error (INL)

The variation in characteristics of tapped transmission line, including length and permittivity, produces nonlinearity.

$$\sigma_{elem} = \frac{\Delta t}{t_d} = \frac{\Delta l}{l} + \frac{1}{2}\frac{\Delta \varepsilon}{\varepsilon} \tag{4}$$

Where $\Delta t / t_d$ is the relative variation in delay of unit transmission line, $\Delta l / l$ is the relative variation in length of unit transmission line, and $\Delta \varepsilon / \varepsilon$ is the relative variation in permittivity of the material.

This can be cumulative when the signal propagates in the transmission line, and the INL is caused by the cumulation. The value of the INL is at its maximum in the end of the transmission line.

$$\sigma(n) = \sigma_{elem} \sqrt{n} \tag{5}$$

Where n is the number of tapped transmission line.

As can be seen, the INL is dependent on the variance in the element delay and the length of the transmission line.

C. Random Error

Measurement precision is affected by random nonsystematic noise. The delay of the signal propagating in the transmission line is affected by noise, as well as the coincidence detection circuits. As is known, the delay caused by the crosstalk between close transmission lines becomes significant when the wiring space is small, especially in the submicron CMOS technology. The start and stop signals can

also have jitter, which give rise to a trigger error for the timing signals.

V. Simulation Result of TDC

A chip is designed in a 0.18-μm standard CMOS process. Using HSpice, a simulation of the chip is performed. 64 segments of tapped transmission lines were fabricated on the chip. Every 16 segments of tapped transmission lines in series are driven by a buffer. The difference of the two tapped transmission line is 1.5mm, the mean value of delay of which is measured to be 37.5ps. It is used as unit delay lines to quantize the time interval. Therefore, the LSB resolution of the interpolation is 37.5ps, and the corresponding quantization noise is calculated to be 15.3ps by (3). Differences exist in the delays of tapped transmission lines, as shown in Fig.7, and they are characterized by σ_{elem}, which is calculated to be 8.6ps.

A systematic error of 370ps exists due to the coincidence detection circuit and can be easily corrected. Since two buffers are inserted for driving the vernier every 16 segments, the difference of delay between the two buffers which is measured to be 230ps should be corrected. The single-shot precision when the time interval is swept over the measurement range from 0 to 2.4ns is presented in Fig. 8. The rms value of the single-shot precision is calculated to be 22.9ps.

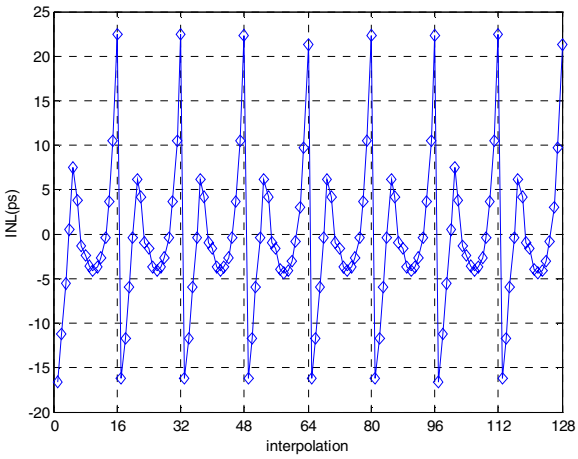


Figure 7. INL of the chip

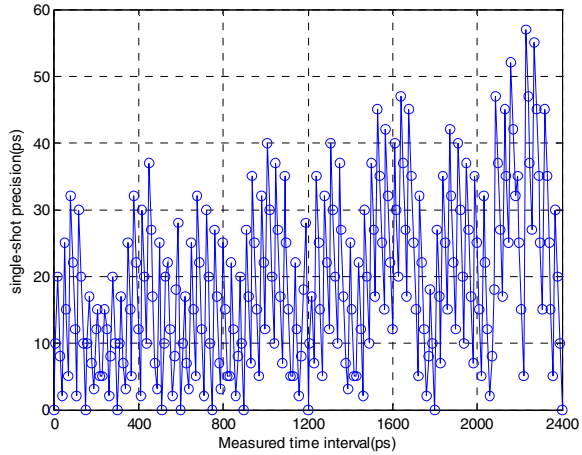


Figure 8. Single-shot precision measured over the measurement range of the chip

VI. Prototype Demonstration

As a demonstration of this principle, a prototype was implemented using 20 segments of microstrip of 5cm in length on a printed-circuit board (PCB) as delay line. The edge-trigger flip-flop of MC10KH family was used as the coincidence detection circuit, while the line receiver are used as buffer to drive every 10 segments of microstrip. The measurement was implemented where the measured time intervals were generated by Agilent 81130Apulse generator, of which the timing resolution is 2ps.

The resolution of the prototype was measured to be 250ps, and the corresponding quantization noise was 102ps, while the INL was shown in Fig. 9 and the standard deviation of INL σ_{elem} was 34ps. The single-shot precision of the prototype when the time interval is swept by steps of 50ps over the measurement range from 0 to 5ns is presented in Fig. 10. The rms value of single-shot precision is calculated to be 108ps at room temperature.

The temperature stability of the prototype was derived from Fig. 2 at temperatures ranging from 0 to 70℃. The temperature drift resulting from the delay offset of the microstrip of 5cm was less than 0.185ps/℃.

Now that the measurement range has been enlarged to 5ns, the measurement range can be further enlarged by using a 200MHz counter.

VII. Conclusion

In this paper, A TDC based on time-space relationship has been presented. A chip is designed in a standard 0.18-um CMOS technology, which presents a resolution and measurement range of 37.5ps and 2.4ns, respectively, in the simulation using HSpice, while the single-shot precision is 22.9ps calculated from the test result.. As a demonstration of the principal, a prototype is implemented using microstrip on PCB. A resolution of 250ps and a measurement range of 5ns are obtained, while the single-shot precision is 108ps calculated from the test result.

Compared to the technique of using logic unit as delay line for time digitizing, using transmission line takes advantages of far higher resolution in potential, since the resolution is equal to the delay of the tapped transmission line. Higher resolutions can be achieved by reduction of the length of transmission line and improvement of coincidence detection circuits. Also, since the transmission line is passive, the noise is lower than active delay unit, that is, the random error is improved. The measurement range can be further enlarged by using counter.

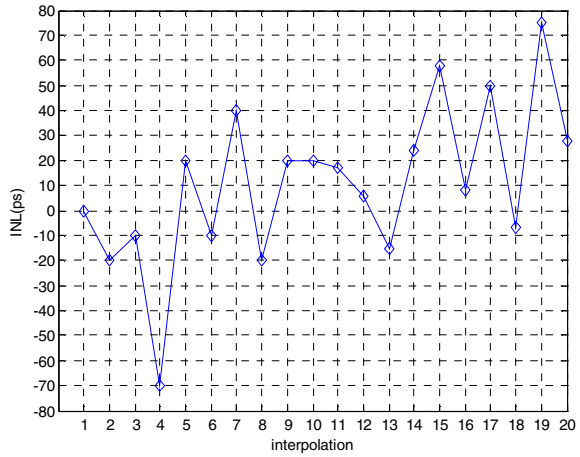


Figure 9. INL of the prototype

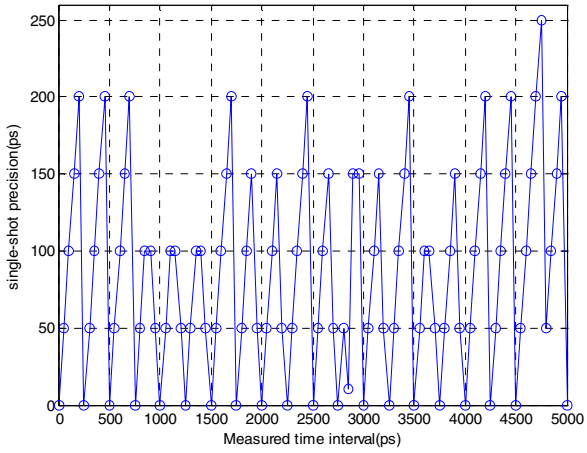


Figure 10. Single-shot precision measured over the measurement range of the prototype

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